Ka-BAND 1 WATT POWER GaAs MMICs

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ABSTRACT

High-power and high-gain Ka-band GaAs MMICs have been developed using a Be co-implantation technique. At 29.5 GHz, an output power of 1 W with 4.2 dB gain has been obtained with gate width of 4.8 mm MMIC. This power gain is the highest value reported to date on Ka-band FETs providing an output power of 1 W. The intercept point of +42 dBm has been obtained from the 3rd order inter-modulation distortion measurements.

INTRODUCTION

Intensive development activities have been forcused on GaAs power FETs to meet high power, high gain demands from satellite communications, phased-array radars, and electronics warfare systems operating at Ka-band. Kobiki et al(1) have reported MMICs providing output power of 1.1 W with 3.0 dB gain, using the source island via hole PHS structure and monolithic power divider/combiner circuits. Recently MMICs with on-chip bias circuits and DC blocking yielding output power of 0.48 W have also been developed by Hung et al(2). These MMICs, however, don't seem to have sufficient power gains for practical use.

The purpose of this paper is to report on high gain Ka-band GaAs FETs with on-chip matching circuits(MMICs) fabricated using Be^+ co-implantation technique. At 29.5 GHz, the developed MMIC with 4.8 mm gate width yielded output power of 1 W with 4.2 dB gain. This gain is the highest value at 1 W output power. The intercept point of + 42 dBm has been obtained from the 3rd order intermodulation distortion measurement. This distortion level is as low as applicable to digital communication systems.

DEVICE STRUCTURES

Fig.1 shows the top view of the 4.8 mm width MMIC chip. The MMIC consists of two unit FET cells combined with low and high transmission lines, which transform low impeadances of FET to high ones. The chip size is 2.1mm x 3.2mm.

It is necessary to attain a very low source inductance for high gain and stable operation in the high frequency range, but the cell dimension should also be kept small to minimize the internal phase and amplitude differences. The source overlay structure(3) was chosen for this purpose. A SEM photograph showing the FET part of an MMIC is shown in Fig.2. The gate fingers are combined by a gate bus bar, and the source fingers are connected by air bridges across the gate bus bar to the source pads. These source pads are grounded by via holes to the PHS placed to the back side of the substrate (via holes not visible). The nominal gate length is 0.6 μm and the unit gate finger length is 50 μm. The average gate to gate spacing is 16 μm.

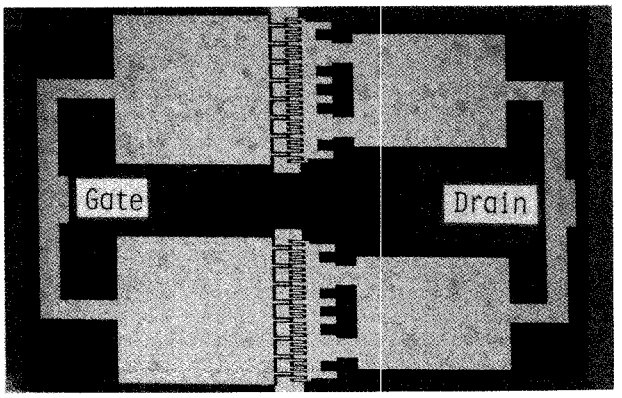

Fig.1 Top view of the 4.8 mm width MMIC

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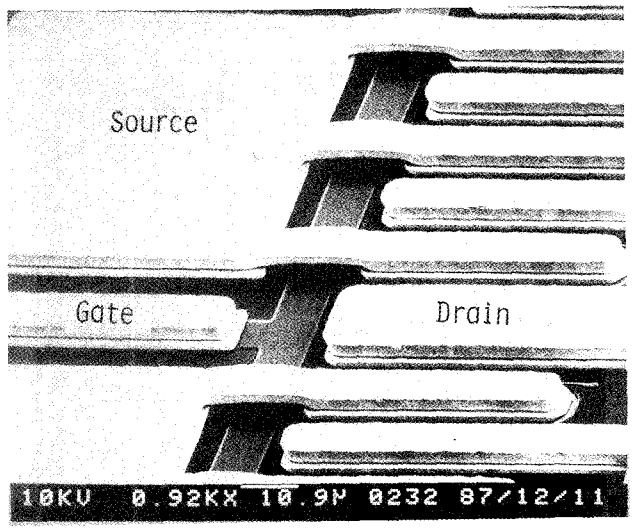

Fig.2 SEM photograph of FET part of the MMIC

In addition to the FET geometry, gate recess width has a significant effect on microwave performance. The recess width was chosen to be 0.9 μm on the basis of a trade-off of small signal gain and saturation power.

WAFER PROCESSING

The starting wafers are 2-inch undoped LEC semi-insulating GaAs substrates. The n-type channel layer is formed by selective co-implantation of Si^+ and Be^+ ions, first Si^+ implant dose of $1.7 \times 10^{12}\ cm^{-2}$ at 150 Kev plus $2 \times 10^{12}\ cm^{-2}$ at 50 Kev, then Be^+ implant dose of $6 \times 10^{11}\ cm^{-2}$ at 130 Kev. Next Si^+ implantations with a dose of $2 \times 10^{13}\ cm^{-2}$ are performed successively at 50, 120, and 250 Kev to form n^+ layers for source and drain. The wafers are capless annealed at 850 °C for 15 min. in pure argon ambient containing a small amount of arsine (AsH_3). The channel layer carrier profile determined by the capacitance-voltage technique is shown in Fig.3, compaired with that without Be^+ co-implant. It is seen that Be^+ co-implant improves the abruptness of carrier profiles, which results in the increase of transconductance near the pinch-off. The source and drain ohmic contacts and the gate electrodes are defined by conventional photolithography and lift-off process. After passivation is done by depositing 2000 A of plasma SiN film, the transmission lines forming internal matching circuits, and pads are defined by electron-beam lithography,

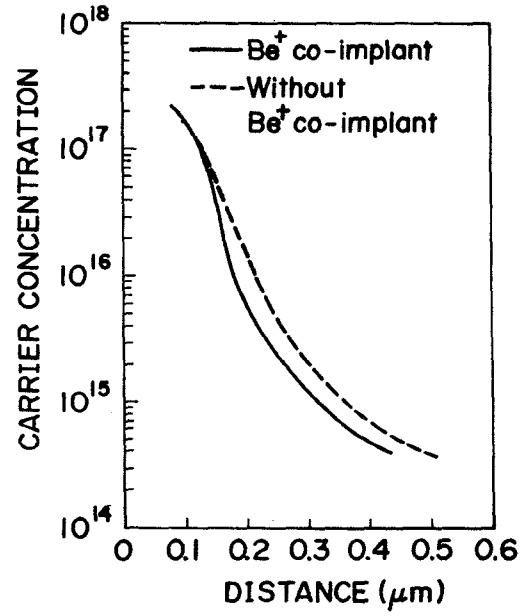

Fig.3 Carrier profiles with and without Be^+ co-implant

followed by selective gold plating with 4 m thickness. Plated air bridges are also formed to connect source and source pads. Then, the wafers are thinned down to 30 ± 5 μm using a combination of lapping technique and chemi-mechanical polishing, and via holes are formed by chemical etching. A 30 μm thick plated gold heatsink interconnects all the via holes.

PERFORMANCE

Typical equivalent circuit for 600 m gate width monitor FET is shown in Fig.4. The drain-to-source voltage and drain current were 7.0 v and 100 mA respectively. The estimated parameters measured under the above bias condition were almost identical between the FET without Be^+ co-implant and the FET with Be^+ co-implant. However, this is not the case under different bias conditions. Table 1 shows the estimated parameters Gm0 , Cgs , Rds and Ri at various drain current levels. For FET without Be^+ co-implant ,Gm0 decreases about 44 % with the decrease of Ids from 100 mA to 35 mA. But as for FET with Be^+ co-implant, Gm0 decrease was only 19 % . These results were attributed to the improved abruptness of carrier profiles by Be^+ co-implant noted previously.

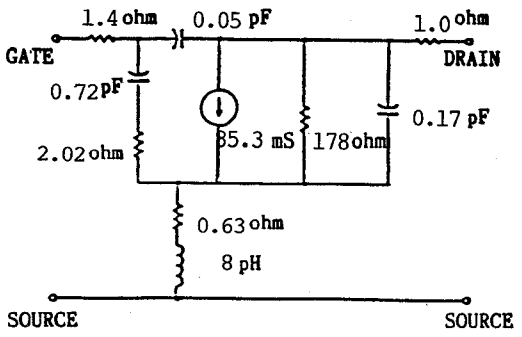

Fig.4 Typical equivalent circuit of the monitor FET (600 μm)

Device	Drain Current (mA)	Gmo (mS)	Cgs (pF)	Rds (Ω)	Ri (Ω)
FET with Be co -implant (Idss= 140mA)	100	85.3	0.72	178	2.02
	70	81.9	0.65	157	2.00
	35	68.7	0.57	151	1.98
FET without Be co -implant (Idss= 148mA)	100	76.6	0.66	158	2.21
	70	64.6	0.57	144	2.21
	35	43.0	0.48	142	2.38

Table 1 Equivalent circuit parameters for various drain current levels

MMICs were dc screened before assembling on a W(80%), Cu(20%) carrier. Typical drain saturation current, pinch-off voltage, and transconductance were 1.5 A(310 mA/mm), -4 V and 580 mS(120 mS/mm), respectively for the 4.8 mm width MMIC. The gate-drain breakdown voltage at a reverse current of 200 μA was typically 14 V.

Microwave performance were measured using test fixtures shown in Fig.5, whose losses were about 0.6 dB. Fig.6 shows output power and power added efficiency vs. input power of the 2.4 mm width (dashed lines) and the 4.8 mm width(solid lines) MMICs. At 29.5 GHz, a power gain of 4.2 dB at the 1 W output power level was obtained with the 4.8 mm width MMIC. The saturation output power was 1.6 W with 3 dB gain. While for the 2.4 mm width MMIC , a power gain of 5.3 dB at the 0.5 W output power level and a Saturation output power of 1 W with 3 dB gain were obtained. The maximum power

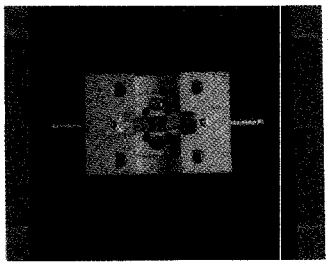

Fig.5 Photograph of the test fixture

added efficiencies were 16 % and 11.7 % for the 2.4 mm and the 4.8 mm width MMICs respectively. The power combining efficiency is about 80 %. Fig.7 shows a typical frequency response of output power of the 2.4 mm and the 4.8 mm width MMICs. Fig.7 shows a typical frequency response of output power of the 2.4 mm and the 4.8 mm width MMICs. An output power higher than 0.5 W with 4 dB gain was obtained over the range of 28.0 - 30.0 GHz for the 2.4 mm width MMIC,while for the 4.8 mm width MMIC, an output power higher than 1 W with 3 dB gain was achieved over the range of 28.9 - 30.0 GHz. The frequency response for the 4.8 mm width MMIC will be improved further by optimization of the on-chip matching circuits. The 3rd order intermodulation distortion(IM_3) was measured for the 4.8 mm width MMIC by the two tone test. The result is shown in Fig.8. The intercept point was +42 dBm, which shows low distortion applicable to digital communication systems.

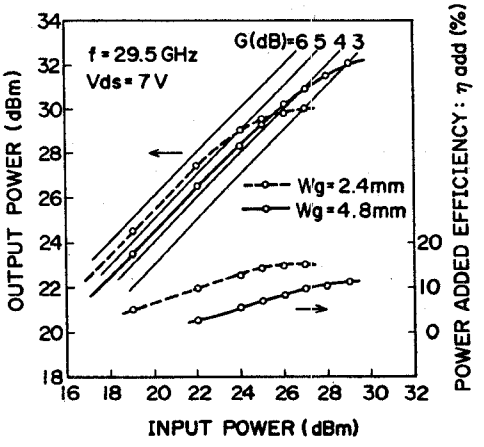

Fig.6 Typical input-output characteristics of the 2.4 mm and 4.8 mm width MMIC

Thermal resistance measurements were carried out by using a infrared microscope. For the 4.8 mm width MMICs, the thermal resistance estimated from the maximum measured temperature was typically 6 °C/W. The channel temperature increase was evaluated to be about 40 °C at 1 W output power operation. It promises a reliable high power operations.

CONCLUSION

High power, high gain Ka-band GaAs MMICs have been developed using a Be^+ co-implantation technique. The 4.8 mm width MMIC delivered CW output power of 1 W with 4.2 dB gain. This power gain is the highest one reported to date on Ka-band FETs providing a output power of 1 W, which makes easier to design the level diagram of Ka-band high power FET amplifiers.

ACNOWLEGEMENT

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REFERENCES

(1) M. Kobiki et al. "A Ka-Band GaAs Power MMIC", IEEE Microwave and Millimeterwave Monolithic Circuits Symposium, Digest of Papers, May. 1985.

(2) H. L. A. Hung et al. "Ka-BAND MONOLITHIC GaAs power FET AMPRIFIRES", IEEE MTT-S International Microwave Simposium Digest, June 1987, pp.89-92.

(3) Y.Hirachi et al. " A Packaged 20 GHz 1W GaAs MES FET with a Novel Via-Hole Plated Heat Sink Structures", IEEE Trans. MTT, vol. MTT-32, No.3, March,1984, pp.309-316

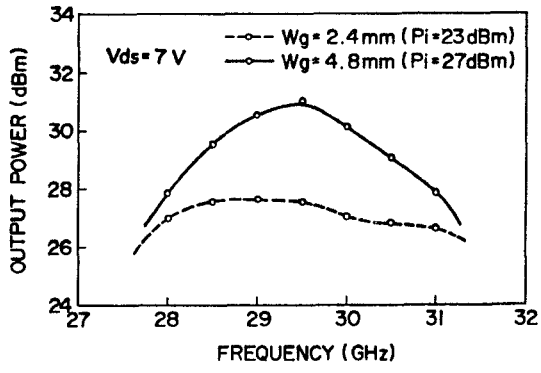

Fig.7 Tipical frequency response of the 2.4 mm and 4.8 mm width MMIC

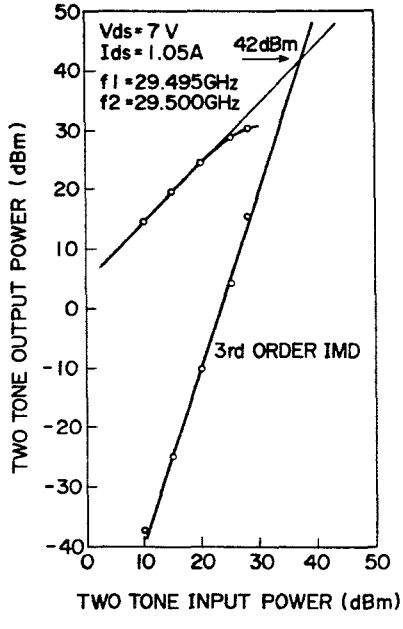

Fig.8 Third order intermodulation characteristics of the 4.8 mm width MMIC